What is claimed is:

1. A capacitor comprising:

an approximately plate-shaped capacitor main body having a first surface on which a semiconductor device having surface-connecting terminals is to be mounted and a second surface; and

a plurality of electrically conductive vias penetrating the capacitor main body between the first and second surfaces for connection with the surface-connecting terminals.

2. A semiconductor device equipped capacitor assembly comprising:

a semiconductor device having surface-connecting terminals; and

a capacitor having an approximately plate-shaped capacitor main body having a first surface on which the semiconductor device is mounted and a second surface and a plurality of electrically conductive vias penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting terminals.

3. A capacitor equipped substrate assembly comprising:

a substrate having surface-connecting pads; and

a capacitor having an approximately plate-shaped capacitor main body having a first surface and a second surface at which the capacitor is mounted on the substrate and a plurality of electrically conductive vias penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting pads.

4. An assembly comprising:

a semiconductor device having surface-connecting terminals;

a substrate having surface-connecting pads; and

a capacitor having an approximately plate-shaped capacitor main body having a first surface on which the semiconductor device is mounted and a second surface at which the capacitor main body is mounted on the substrate and a plurality of electrically conductive vias penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting terminals and the surface-connecting pads.

5. An interposer comprising:

an interposer main body having a first surface on which a semiconductor device having surface-connecting terminals is mounted and a second surface formed with a recess;

a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between the first surface and a bottom surface of the recess and connected to the surface-connecting terminals; and

a capacitor disposed in the recess and having front and rear surfaces and a plurality of capacitor side electrically conductive vias passing through the front and rear surfaces and connected to the interposer main body side electrically conductive vias.

6. An interposer according to claim 5, further comprising, within the interposer main body, a plurality of short electrically conductive ground vias

passing through the first surface and an electrically conductive via pitch changing layer, at least a part of the short electrically conductive ground vias being electrically connected to ground vias of the capacitor side electrically conductive vias by way of the electrically conductive via pitch-changing layer.

7. An interposer according to claim 5, further comprising, within the interposer main body, a plurality of short electrically conductive power vias passing through the first surface and an electrically conductive via pitch-changing layer, at least a part of the short electrically conductive power vias being electrically connected to power vias of the capacitor side electrically conductive vias by way of the electrically conductive via pitch-changing layer.

8. A semiconductor device equipped interposer assembly comprising:

a semiconductor device having surface-connecting terminals; and

an interposer having an approximately plate-shaped interposer main body having a first surface on which the semiconductor device having surface-connecting terminals is mounted and a second surface formed with a recess, a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between the first surface and a bottom surface of the recess and connected to the surface-connecting terminals, and a capacitor disposed in the recess and having front and rear surfaces and a plurality of capacitor side electrically conductive vias extending through the front and rear surfaces and

connected to the interposer main body side electrically conductive vias.

9. An interposer equipped substrate assembly comprising:

a substrate having surface-connecting terminals; and

an interposer having an approximately plate-shaped interposer main body having a first surface and a second surface formed with a recess, the interposer main body being mounted at the second surface on the substrate, the interposer further having a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between the first and second surfaces and connected to the surface-connecting terminals and a capacitor disposed in the recess and having front and rear surfaces and a plurality of capacitor side electrically conductive vias passing through the front and rear surfaces and connected to the interposer main body side electrically conductive vias.

10. An assembly comprising:

a semiconductor device having surface-connecting terminals;

a substrate having surface-connecting pads; and

an interposer having an approximately plate-shaped interposer main body having a first surface on which the semiconductor device is mounted and a second surface formed with a recess, the interposer main body being mounted at the second surface on the substrate, the interposer further having a plurality of interposer main body side electrically conductive vias

penetrating the interposer main body between the first surface and a bottom surface of the recess and connected to the surface-connecting terminals and a capacitor disposed in the recess and having front and rear surfaces and a plurality of capacitor side electrically conductive vias passing through the front and rear surfaces and connected to the interposer main body side electrically conductive vias and the surface connecting pads.

11. An interposer for electrical connection between a semiconductor device and a package in which the semiconductor device is mounted, comprising:

a capacitor portion having a dielectric layer between inner layer electrodes; and

a surrounding portion surrounding a lateral periphery of the capacitor portion and made of a material having a thermal expansion coefficient smaller than that of the dielectric layer.

12. An interposer according to claim 11, wherein the capacitor portion is configured so as to surround all of the lateral periphery of the capacitor portion.

13. An interposer according to claim 12, wherein the surrounding portion is made of a material having a thermal expansion coefficient of 10 ppm/℃ or smaller.

14. An interposer according to claim 13, wherein the surrounding portion is made of alumina.

15. An interposer according to claim 11, further comprising a wiring for electrical connection between

the IC device and the package, at least part of the wiring being disposed so as to penetrate the surrounding portion.

16. An interposer according to claim 15, wherein the surrounding portion is made of a material having a specific inductive capacity smaller than that of the dielectric layer.

17. A semiconductor device equipped interposer assembly comprising:

a semiconductor device; and

an interposer having a wiring electrically connected to the semiconductor device;

the interposer including a capacitor portion having a dielectric layer between inner layer electrodes, and a surrounding portion surrounding a lateral periphery of the capacitor portion and made of a material having a thermal expansion coefficient smaller than that of the dielectric layer.

18. An interposer equipped package assembly comprising:

an interposer having a wiring; and

a package electrically connected to the wiring of the interposer;

the interposer having a capacitor portion having a dielectric layer between inner layer electrodes, and a surrounding portion surrounding a lateral periphery of the capacitor portion and made of a material having a thermal expansion coefficient smaller than that of the dielectric layer.

19. An assembly comprising:

a semiconductor device;

a package in which the semiconductor device is mounted; and

an interposer interposed between the semiconductor device and the package and connecting therebetween;

the interposer including a capacitor portion having a dielectric layer between inner layer electrodes, and a surrounding portion surrounding a lateral periphery of the capacitor portion and made of a material having a thermal expansion coefficient smaller than that of the dielectric layer.

20. A method of producing an interposer for electrical connection between a semiconductor device and a package in which the semiconductor device is mounted, the interposer including a capacitor portion having a dielectric layer between inner layer electrodes, the method comprising:

forming a surrounding portion that surrounds the capacitor portion from a material having a thermal expansion coefficient smaller than that of the dielectric layer.

21. A method according to claim 20, wherein the forming of the surrounding portion comprises forming the surrounding portion integrally with the capacitor portion.

22. A method according to claim 20, wherein the forming of the surrounding portion comprises fitting the capacitor portion in the surrounding portion.